Table 1: Seal5 LLVM patch phases and their default assignments.

Phase	Purpose	Default contents
`PHASE_0`	Bootstrap support	Insertion markers, PatternGen integration, and supporting backend changes.
`PHASE_1`	Structural integration	TableGen include scaffolding, ISA information, intrinsics, and GlobalISel legalizer integration.
`PHASE_2`	Instruction integration	Features, register definitions, operand field types, instruction definitions, and disassembler integration.
`PHASE_3`	Custom patches	No assignment from the currently registered generators; available to configured patches.
`PHASE_4`	Selection patterns	PatternGen-generated instruction-selection rules and associated artifacts.
`PHASE_5`	Custom patches	No assignment from the currently registered generators; available to configured patches.

Phases are applied in numeric order. These are default assignments; configuration can add or replace patches in any phase.